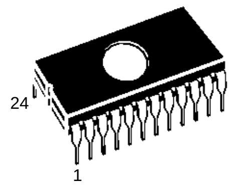
NMOS 32K (4K x 8) UV EPROM

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 35mA max
- INPUTS and OUTPUTS TTL COMPATIBLE DURING READ and PROGRAM
- COMPLETELY STATIC



FDIP24W (F)

DESCRIPTION

The M2732A is a 32,768 bit UV erasable and electrically programmable memory EPROM. It is organized as 4,096 words by 8 bits. The M2732A with its single 5V power supply and with an access time of 200 ns, is ideal suited for applications where fast turn around and pattern experimentation one important requirements.

The M2732A is honsed in a 24 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can be then written to the clerice by following the programming procedure.

Table 1. Signal Names

A0 - A11	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

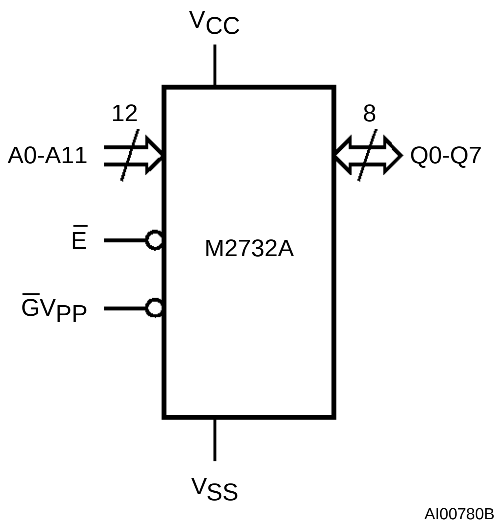
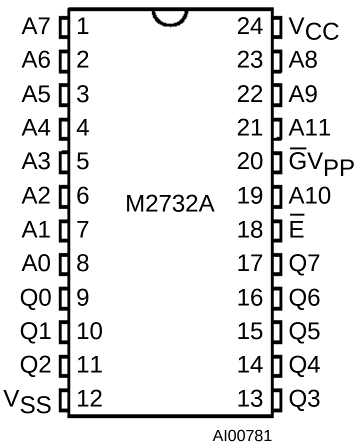


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6	V
V_{CC}	Supply Voltage		–0.6 to 6	V
V_{PP}	Program Supply Voltage		–0.6 to 22	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The six modes of operation for the M2732A are listed in the Operating Modes Table. A single 5V power supply is required in the read mode. All inputs are TTL level except for V_{PP}.

Read Mode

The M2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{AVAQ}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M2732A has a standby mode which reduces the active power current by 70 %, from 125 mA to 35 mA. The M2732A is placed in the standby mode by applying a TTL high signal to $\overline{E}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because M2732A's are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{E}$ be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

Programming

When delivered, and after each erasure, all bits of the M2732A are in the “1” state. Data is introduced by selectively programming ”0’s” into the desired bit locations. Although only “0’s” will be programmed, both “1’s” and “0’s” can be presented in the data word. The only way to change a “0” to a ”1” is by ultraviolet light erasure.

The M2732A is in the programming mode when the $\overline{G}V_{PP}$ input is at 21V. A 0.1µF capacitor must be placed across $\overline{G}V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied, 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50ms, active low, TTL program pulse is applied to the $\overline{E}$ input. A program pulse must be applied at each address location to be programmed. Any location can be programmed at any time - either individually, sequentially, or at random. The program pulse has a maximum width of 55ms. The M2732A must not be programmed with a DC signal applied to the $\overline{E}$ input.

Programming of multiple M2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Inputs of the paralleled M2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{E}$ input programs the paralleled 2732As.

Program Inhibit

Programming of multiple M2732As in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}V_{PP}$) of the parallel M2732As may be common. A TTL level program pulse applied to a M2732A’s $\overline{E}$ input with $\overline{G}V_{PP}$ at 21V will program that M2732A. A high level $\overline{E}$ input inhibits the other M2732As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is carried out with $\overline{G}V_{PP}$ and $\overline{E}$ at V_{IL}.

ERASURE OPERATION

The erasure characteristics of the M2732A are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M2732A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to the direct sunlight. If the M2732A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M2732A window to prevent unintentional erasure.

The recommended erasure procedure for the M2732A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M2732A should be placed within 2.5 cm of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	V_{CC}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{CC}	Data Out
Program	V_{IL} Pulse	V_{PP}	V_{CC}	Data In
Verify	V_{IL}	V_{IL}	V_{CC}	Data Out
Program Inhibit	V_{IH}	V_{PP}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Note: X = V_{IH} or V_{IL}.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

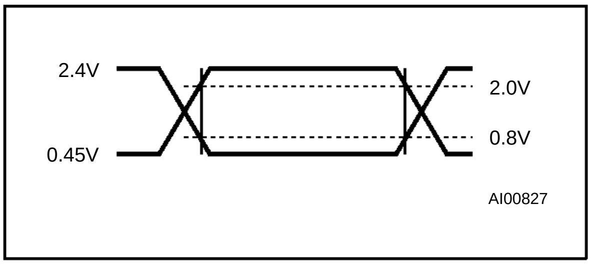


Figure 4. AC Testing Load Circuit

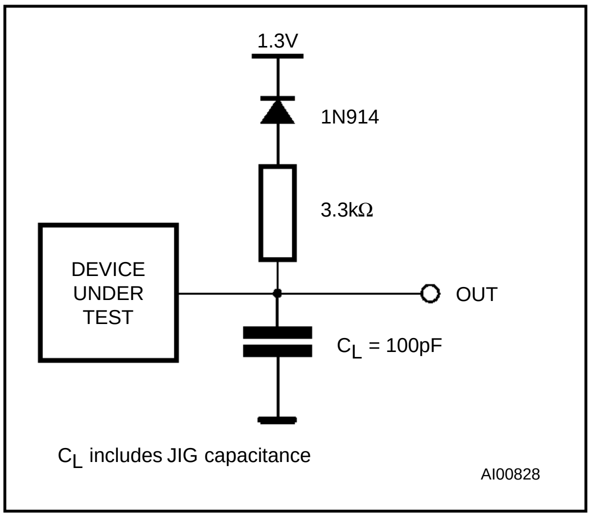


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (except $\overline{G}V_{PP}$)	V_{IN} = 0V		6	pF
C_{IN1}	Input Capacitance ($\overline{G}V_{PP}$)	V_{IN} = 0V		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

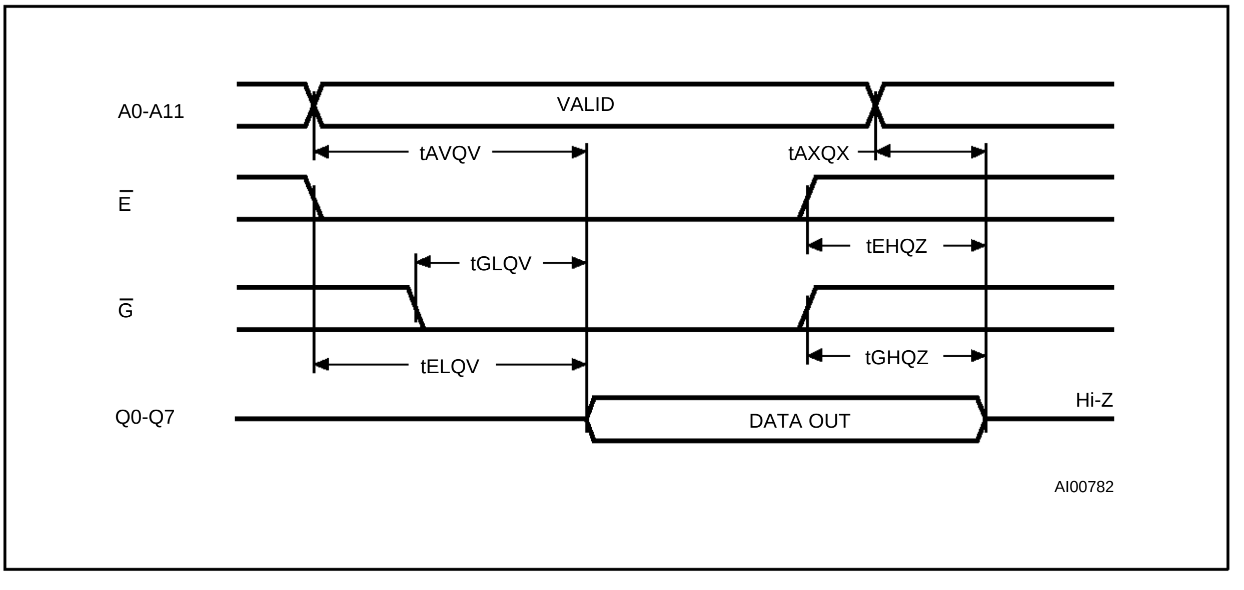


Table 5. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Value		Unit
			Min	Max	
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		125	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$, $\overline{G} = V_{IL}$		35	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 6. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M2732A								Unit
				-2, -20		blank, -25		-3		-4		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		200		250		300		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250		300		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		100		100		150		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	60	0	60	0	130	0	130	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	60	0	60	0	130	0	130	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Table 7. Programming Mode DC Characteristics [1]
(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 21V ± 0.5V)

Symbol	Parameter	Test Condition	Min	Max	Units
I_{LI}	Input Leakage Current	$V_{IL} \leq V_{IN} \leq V_{IH}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		125	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{PP}$		30	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

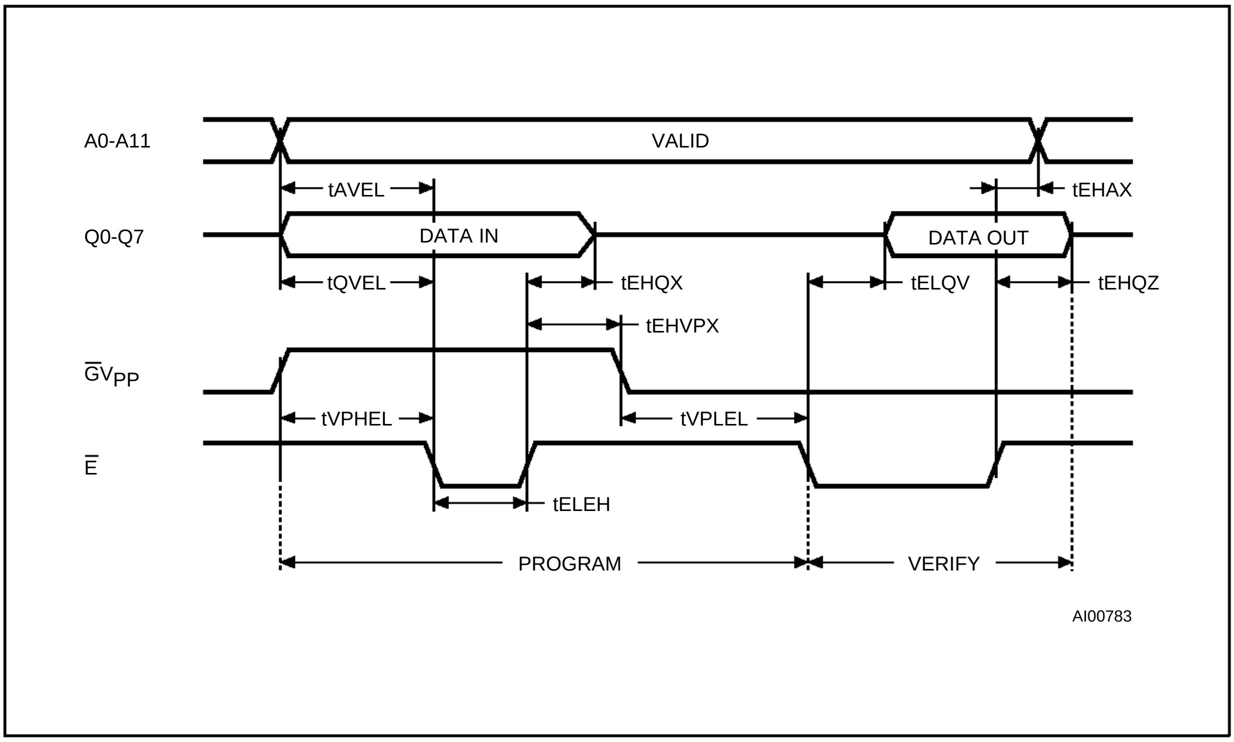
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 8. Programming Mode AC Characteristics [1]
(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 21V ± 0.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
$t_{VPL1VPL2}$	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		45	55	ms
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		1	µs
t_{EHQZ}	t_{DF}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Figure 6. Programming and Verify Modes AC Waveforms



ORDERING INFORMATION SCHEME

Example: M2732A -2 F 1

Speed and V_{CC} Tolerance	
-2	200 ns, 5V ±5%
blank	250 ns, 5V ±5%
-3	300 ns, 5V ±5%
-4	450 ns, 5V ±5%
-20	200 ns, 5V ±10%
-25	250 ns, 5V ±10%

Package	
F	FDIP24W

Temperature Range	
1	0 to 70 °C
6	–40 to 85 °C

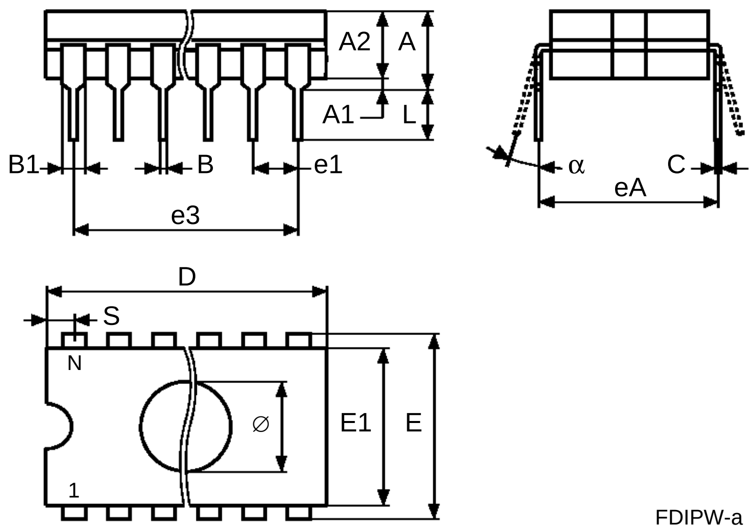
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP24W - 24 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			32.30			1.272
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	–	–	0.100	–	–
e3	27.94	–	–	1.100	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	7.11	–	–	0.280	–	–
α		4°	15°		4°	15°
N	24			24		

FDIP24W



Drawing is not to scale